BEST AVAILABLE IMAGES

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images may include (but are not limited to):

- BLACK BORDERS
- TEXT CUT OFF AT TOP, BOTTOM OR SIDES
- FADED TEXT
- ILLEGIBLE TEXT
- SKEWED/SLANTED IMAGES
- COLORED PHOTOS
- BLACK OR VERY BLACK AND WHITE DARK PHOTOS
- GRAY SCALE DOCUMENTS

IMAGES ARE BEST AVAILABLE COPY.

As rescanning documents *will not* correct images, please do not report the images to the Image Problem Mailbox.

REMARKS

The above Amendments and these Remarks are in reply to the Office Action mailed May 21, 2003. Claims, 70-81, 94-95 and 101-122 are pending in the application. Claims 101-122 are new.

I. Amendment to the Specification

Applicants have amended the specification to add a new paragraph. The new paragraph is not new matter. Rather, the new paragraph is based on originally filed claims 13 and 25.

II. New Claims 101-122

The Examiner rejected the originally filed claims under 35 U.S.C. §102 as being anticipated by *Boyle et al.* (U.S. Patent 6,557,145).

Applicant now adds new claims 101-122 to better cover various embodiments. To help the Examiner, Applicants will distinguish new claims 101-122 from *Boyle et al.*

New claims 101-122 are patentable over *Boyle et al.* because *Boyle et al.* dos not disclose all of the limitations of the new claims.

Traditionally, gate level net lists have been generated by logic synthesis tools from RTL descriptions. "Previous logic synthesis tools are problematic because they generate net lists without sufficient physical layout information. Since wire delays account for such a large proportion of the total delays with deep sub-micron designs, these logic synthesis tools invariably generate sub-optimal net lists. Consequently designers using these tools are often required to perform numerous iterations of the above-defined design sequence, each consuming potentially many weeks or more, before timing problems created using sub-optimal net lists can be corrected." [Specification, pp. 3-4].

One embodiment of the present invention solves this problem by creating a physical prototype based on the net list, prior to creating the physical design. The physical prototype "provides a forward prediction of the area, timing and performance of the final GDS of the design generated by a physical implementation tool." [Specification, p. 4]. For example, Figure 1 depicts "a front-end logic design stage 12 and a back-end physical design stage 14." [Specification, p. 4]. The physical prototype is created during the front-end logic design stage

12 and then is provided to the back-end physical design stage 14. The back-end physical design stage 14 includes a physical implementation tool that creates the physical design based on the physical prototype. Variations of the above described embodiment are recited in the new claims. For example, claim 101 recites:

> 101. (new) A method of performing a design of a circuit, comprising:
>
> accessing a gate level design for said circuit;
>
> creating a physical prototype from said gate level design, said creating of a physical prototype includes predicting of timing for said circuit and tracking an error in said predicting of timing; and
>
> creating a physical design for said circuit, said creating of said physical design includes placing and routing elements of said circuit, said creating of a physical prototype is performed prior to said creating of said physical design.

The cited prior art does not disclose "creating a physical prototype ... and creating a physical design for said circuit, ... said creating of a physical prototype is performed prior to said creating of said physical design." There is no disclosure in *Boyle et al.* of creating a physical prototype prior to creating the physical design, as recited above in claim 101.

Boyle et al. pertains to "a method for optimizing a layout design, which minimizes the optimization cycle by incorporating interconnect wiring delays and performing logic optimization in the placement and routing operations." [*Boyle et al.* col. 3, lines 23-26]. Looking at Figures 1 and 2 of *Boyle et al.*, the disclosure of *Boyle et al.* is concerned with placement, and routing – see box 250 of Fig. 2. Figure 3 of *Boyle et al.* provides further details of how the optimized placement and routing is performed. This placement and routing described by *Boyle et al.* is analogous to the physical implementation tool that creates the physical design in the present application. Thus, *Boyle et al.* does disclose creating a physical design. However,

Boyle et al. does not disclose "creating of a physical prototype ... prior to said creating of said physical design" as recited in claim 101.

Because *Boyle et al.* does not disclose all of the limitations of claim 101, Applicants assert that claim 101 is patentable over the cited prior art. For the same reasons as discussed above with respect to claim 101, Applicants assert that claims 102-122 are also patentable over the cited prior art.

III. Claims 70-81

The Examiner rejected claims 70-81 under 35 U.S.C. §102 as being anticipated by *Boyle et al.* Because *Boyle et al.* does not disclose all of the limitations of claims 70-81, Applicants assert that the claims are in condition for allowance.

Claim 70 recites the receiving of a prototype and creating a physical design based on the prototype. Thus, for the same reasons as discussed above with respect to claim 101, Applicants assert that claims 70-75 are patentable over the cited prior art.

Claim 76 recites a semiconductor device manufactured by the receiving of a prototype and creating a physical design based on the prototype. Thus, for the same reasons as discussed above with respect to claim 101, Applicants assert that claims 76-81 are patentable over the cited prior art.

IV. Claims 94-95

The Examiner rejected claims 94-95 under 35 U.S.C. §102 as being anticipated by *Boyle et al.* However, because *Boyle et al.* dos not disclose all of the limitations of the claims 94-95, Applicants assert that these claims are in condition for allowance.

Claim 94 recites that a first bin has "a first group of nets optimized to a first set of criteria ... a second bin [has] a second group of nets optimized to a second set of criteria, wherein the first criteria and the second criteria are substantially different." For example, page 12 of the specification states:

> Referring to Figure 7, a diagram that illustrates an integrated circuit that has been designed and fabricated according to the present invention is shown. The integrated circuit 90 includes a plurality of bins 92. Assuming in this example that the

> prototype optimization tool 50 was used with certain bins (i.e., bin 92a and 92b), the optimization criteria for both of these bins is different than the other bins where optimization was not needed. In other words, the bins 92 are designed to a criterion of O, the bin 92a was designed to a criterion of O' and the bin 92b was designed to yet another criterion of O''. Since each optimization criterion is different, one or more nets in the bins 92, 92a and 92b are therefore optimized to different criteria respectively.

The Examiner asserted that above quoted limitations from claim 94 are found in *Boyle et al.* at col. 1, lines 24-27; col. 6, lines 50-65; col. 9, lines 40-67; col. 10, lines 1-6; col. 11, lines 9-40; col. 11 lines 63-67; col. 12, lines 1-5; and col. 14, lines 20-56. Applicants have reviewed the cited portions of *Boyle et al.* and assert that those cited portions do not disclose the limitations of claim 94. Each of the cited portions are described below.

a. col. 1, lines 24-27

This is the field of the invention. There is no mention of different groups or different criteria.

b. col. 6, lines 50-65

Explains how dividing the circuit into clusters improves performance. There is no mention of different criteria.

c. col. 9, lines 40-67

Describes that the circuit is divided into bins. There is no mention of different criteria for different bins.

d. col. 10, lines 1-6

Describes inter-bin wires. There is no mention of different criteria for different bins.

e. col. 11, lines 9-40

Describes performance of nets in clusters. There is no mention of different criteria for different bins.

f. col. 11 lines 63-67 and col. 12, lines 1-5

Describes delays of nets. There is no mention is different criteria for different bins.

g. col. 14, lines 20-56

In the first paragraph, congestion is discussed. The second paragraph describes dividing into bins. However, there is no disclosure of different criteria for different bins.

As demonstrated, none of the passages cited by the Examiner disclose "that a first bin has "a first group of nets optimized to a first set of criteria ... a second bin [has] a second group of nets optimized to a second set of criteria, wherein the first criteria and the second criteria are substantially different." Therefore, claim 94 is not anticipated by *Boyle et al.*

By reason of its dependency on claim 94, Applicants assert that claim 95 is also patentable over the cited prior art.

In view of the above Amendments and Remarks, reconsideration of claims 70-81 and 94-95 and consideration of new claims 101-122 is requested.

The Commissioner is authorized to charge any underpayment or credit any overpayment to Deposit Account No. 501826 for any matter in connection with this document, including any fee for extension of time, which may be requested.

Respectfully submitted,

Date: August 7, 2003 By: _____

Burt Magen
Reg. No. 37,175

VIERRA MAGEN MARCUS HARMON & DENIRO LLP
685 Market Street, Suite 540
San Francisco, California 94105
Telephone: 415.369.9660
Facsimile: 415.369.9665